Implementation and Algorithms for the FPD DSM Tree 2006 Sums for FPD-East and FPD++

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Description: The first two layers of DSM boards build the ADC sum for each of the 8 detector modules. All these sums are available in the third layer, which sets various thresholds on each sum. The 4 FPD-East modules share 3 common thresholds and a 4th threshold is set on the sum of the North-East and South-East modules. There are 6 thresholds for several different combinations of the FPD++ modules. 8 bits are then sent to the last DSM; 3 from FPD-East and 5 from FPD++. In parallel 13 threshold bits are sent to the scaler boards.

1. FPD++-layer0, FPW-FW001, 002, 003, 005, 006, 007, 008, 009, 010, 011 and FPD East-layer0, FPE-FE001, 002, 003, 005, 006, 007

Input: 16 8-bit ADC values

Registers: None

LUT: Pedestal subtraction

Action:

1st Clock:	Latch input
2nd Clock:	Form intermediate sums
3rd Clock:	Add intermediate sums to 12-bit total sum
4th Clock:	Latch output

Output (0-11) ADC sum,
(12-15) empty

2. FPD++-layer0, FPW-FW004 and FPD-East-layer0, FPE-FE004

Input: 2x7 8-bit ADC values; split module
Ch0-6 First sum
Ch7-13 Second sum
Ch14-15 Unused

Registers: None

LUT: Pedestal subtraction

Action:

1st Clock:	Latch input
2nd Clock:	Form intermediate sums

3rd Clock: Add intermediate sums to 11-bit total sum separately for channels 0-6 and channels 7-13

4th Clock: Latch output

Output (2 cables)
Lower bits First Sum
(0-10) ADC sum
(11-15) empty
Upper bits Second Sum
(16-26) ADC sum
(27-31) empty

3. FPD East-layer0, FPE-FE008, 010

Input: 15 8-bit ADC values from the Top/Bottom Modules

Registers: None

LUT: Pedestal subtraction

Action:
Same as FW001 above, except sums 15 channels instead of 16

Output (0-11) ADC sum,
(12-15) empty

4. FPD-East-layer0, FPE-FE009-011

Input: 10 8-bit ADC values from Top/Bottom modules

Registers: None

LUT: Pedestal subtraction

Action: Same as FW001 above, except sums 10 channels instead of 16

Output (0-11) ADC sum
(12-15) empty

5. FPD++-layer1, FPW-FW101 and FPD-East-layer1, FPE-FE101

Input: 8 ADC sums: 6 12-bit sums and 2 11-bit sums

Registers: **FPW and FPE**: Index 23
R0: Module mask (8)
This is a bit mask for the 8 inputs. For each input/bit: 0 => do not use this input in the sums logic, 1 => do use this input in the sum logic

LUT: 1:1

Action:

1st Clock: Latch input
2nd Clock: Zero out those inputs whose bit in R0 is 0 and then form intermediate sums
3rd Clock: Add intermediate sums to 14-bit module sums separately for inputs 0-3 and inputs 4-7.
4th Clock: Latch output

Output (2 cables)
Lower bits: sum of channels 0-3
(0-13) ADC sum
(14-15) empty
Upper bits: sum of channels 4-7
(16-29) ADC sum
(30-31) empty

6. FPD++-layer1, FPW-FW102 and FPD-East-layer1, FPE-FE102

Input: 4 12-bit ADC sums:

Registers: **FPW and FPE**: Index 28
R0: Module mask (4)
This is a bit mask for the 4 inputs. For each input/bit: 0 => do not use this input in the sums logic, 1 => do use this input in the sum logic

LUT: 1:1

Action:
1st Clock: Latch input
2nd Clock: Zero out those inputs whose bit is 0 in R0 and then add inputs 0-1 and 2-3 separately to form 2 13-bit sums
3rd Clock: Delay output
4th Clock: Latch output

Output (2 cables)
Lower bits: sum of channels 0-1
(0-12) ADC sum
(13-15) empty
Upper bits: sum of channels 2-3
(16-28) ADC sum
(29-31) empty

7. FPD-layer2, L1-FP201

NOTE: This algorithm now uses 4 override cycles to make time to compute all the large sums and do the threshold comparisons. To compensate for the extra time 1 of the 2 blanks in the output FIFO was removed.

Input: One ADC sum per detector module
ch0: East-North
ch1: East-South
ch2: East-Top

ch3: East-Bottom
ch4: FPD++ S1
ch5: FPD++ S2
ch6: FPD++ S3
ch7: FPD++ S4

Registers: **L1**: index: 30

R0: East ADC-threshold 0 (14)
R1: East ADC-threshold 1 (14)
R2: East ADC-threshold 2 (14)
R3: S3, S4-threshold 0 (14)
R4: S13, S24-threshold 0 (15)
R5: S1, S2-threshold 0 (14)
R6: S3, S4-threshold 1 (14)
R7: S13, S24-threshold 1 (15)
R8: S1234-threshold 0 (16)
R9: Sum_E threshold 0 (15)

LUT: 1:1

Action:

1st Clock:	Latch input
2nd Clock:	Place 3 thresholds (R0, R1, R2) on each of the 4 East inputs. Compare S1 and S2 to R5 Compare S3 and S4 to both R3 and R6 Form sum Sum_E = East-North + East-South Form sums S13 = S1 + S3 and S24 = S2 + S4
3rd Clock:	Compare S13 and S24 to both R4 and R7 Compare Sum_E to R9 Form sum S1234 = S13 + S24
4th Clock:	Compare S1234 to R8
5th-6th Clock:	Delay output of all previous clock ticks by the correct amount so all threshold bits arrive at the 7th clock at the same time.
7th Clock:	Combine threshold bits to form desired trigger bits and scaler bits (see output list below)
8th Clock:	Latch output

Output (2 cables)

Lower bits to last DSM LD301
(0) S3 > R3 or S4 > R3
(1) S13 > R4 or S24 > R4
(2) S1 > R5 or S2 > R5
(3) S3 > R6 or S4 > R6
(4) S13 > R7 and S24 > R7 and S1234 > R8

(5) Any FPD-East module > R1
(6) Any FPD-East module > R2
(7) NE > R0 and SE > R0 and Sum_E > R9

(8-15) empty

Upper bits to FPD scaler
(0) NE > R1
(1) SE > R1
(2) NE > R2
(3) SE > R2
(4) NE > R0 and SE > R0 and Sum_E > R9

(5) S3 > R3
(6) S4 > R3
(7) S13 > R4
(8) S24 > R4
(9) S1 > R5
(10) S2 > R5
(11) S3 > R6
(12) S4 > R6
(13) S13 > R7 and S24 > R7 and S1234 > R8

(14-15) empty